REMARKS

The present application includes claims 8-21. Claims 8-21 were rejected by the Examiner.

Claims 8-18 were rejected under 35 U.S.C. 102 as being anticipated by Patel (U.S. Patent No. 4,945,538).

Claims 19-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Patel in view of Huber (U.S. Patent No. 5,107,379).

Claim 21 was rejected under 35 U.S.C. 103(a) as being unpatentable over Patel in view of White (U.S. Patent No. 4,724,496).

The Applicant first turns to the rejection of claims 8-18 in view of Patel. Patel provides for basic processing of an incoming analog signal to generate digital values representative of binary data. Abstract. In Patel, a state-dependent sequence detection algorithm precomputes digital sample values for a preselected number of bits ahead of the current bit, and those values are compared against corresponding thresholds to provide binary decision outputs to determine the next state. Abstract. The thresholds of the decoder are programmable. Abstract.

However, the disclosure of Patel lacks several elements recited in the pending claims of the present application. For example, the system of Patel does not include timing recovery circuitry responsive to both digitized read signals and output of a digital peak detector. This limitation is recited in independent claims 8, 10 and 14 of the present

application. Rather, Patel shows a phase-locked clock 13 which receives a single filtered input based on a coded analog read signal. See Fig. 1 and col. 3, lines 4-7.

Additionally, the system of Patel fails to disclose an RLL (d,k) decoder for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector or providing a run length limited output by decoding a sequence of binary digital signals from the digital peak detector. This limitation is recited in independent claims 8, 10 and 14 of the present application. Rather, the decoder of Patel is deficient in multiple aspects: 1) rather than a variable (d,k) RLL decoder, Patel only discloses an RLL (1,7) fixed decoder; 2) the RLL (1,7) decoder of Patel only receives equalized digitized sample values rather than the dual input provided in the claims of the present application. See Fig. 1 and col. 3 lines 1-2, 26-32 and 45-54.

Furthermore, as previously stated by the Examiner, claims 10 and 14 are allowable over the cited art. In addition to the limitations discussed above, claim 10 recites a delay means for delaying the coupling of the digitized read signals to the digital peak detector or the timing recovery circuit to match the delay of the coupling of the digitized read signals to the timing recovery circuitry or the digital peak detector, respectively, imposed by the digital pulse shaping filter. While Patel mentions a delay 20, the delay provides delay alignment between the analog input signal and clock signal inputs to the analog-to-digital converter (ADC) 21. See Fig. 1 and col. 3, lines 33-43. The Patel delay means 20 only provides a delay before the analog signal reaches the ADC 21, whereas the delay means recited in claim 10 of the present application provides a delay for both the digital peak detector and the timing recovery circuit.

In claim 14, which the Examiner previously indicated was allowable, the sequence detector processes two digitized read signals at a time. However, the circuit of Patel (See Fig. 1) only processes one digitized read signal at a time. Col. 3, lines 33-54.

With regard to the dependent claims, for example, claim 11 recites variable filter parameters for the digital pulse shaping filter circuitry. However, Patel does not disclose variable filter parameters. In fact, Patel states that the filter 12 cannot compensate for anomalies in the signal. Col. 6, lines 39-42 and col. 7, lines 13-18. The decoder of Patel is programmable with different thresholds, but not the filter. Claim 12 of the present application recites a programmable filter and is similarly novel over the disclosure of Patel. Claim 15 recites that the sequence detector allows selection between center and side sampling of the digitized read signals. While Patel shows a read response in Fig. 2B, Patel discusses nothing about selection between center and side sampling of the digitized read signals at the sequence detector.

Thus, there are clearly several differences between Patel and the claims of the present application. In light of those novel differences, such as the differences discussed above, the Applicant respectfully submits that the independent claims 8, 10 and 14 of the present application, as well as their dependent claims 9, 11-13 and 15-21, should be allowable.

The Applicant next turns to the rejection of claims 19-20 over Patel in view of Huber. The Huber '379 patent relates to reducing intersymbol interference by slimming the rising edge and slurring the falling edge of an isolated input magnetic pulse and

providing feedback to produce a compensating waveform that is substantially complimentary to a certain portion (occurring after Tmin) of the filtered waveform. (Abstract; col. 2, lines 38-44.) The complimentary waveform is then added to the filtered waveform to produce a waveform that is substantially a step function. (Abstract; col. 2, lines 45-60.) In Huber '379, a read waveform is processed to determine the presence or absence of a transition within each signaling element. (col. 7, lines 45-48.) The available time window for detection, called the data bit cell or detent time, is completely determined by the rate of the modulation code used. (col. 7, lines 48-50; col. 8, lines 49-61.) The Huber '379 patent does not discuss a digital peak detector, a sequence detector, or an RLL decoder as recited in the pending claims of the present application. The Huber '379 patent does not provide sufficient disclosure regarding a programmable timing recovery circuit to be implemented in the circuit of Patel. Col. 8, lines 49-61. Thus, the teachings of the Huber '379 patent do not cure the deficiencies of the Patel patent with respect to the claimed integrated circuit synchronous read channel of the present application, and claims 19-20 should be allowable.

The Applicant last turns to the rejection of claim 21 over Patel in view of White. White relates to a peak detector to generate a binary waveform. Abstract. While White mentions that time displacement errors may act directly on data or indirectly on clock signals, White provides no enabling disclosure for a timing recovery circuit that computes timing error at transition times. Col. 3, lines 10-21. A general statement of time displacement errors does not serve to provide disclosure of a timing recovery circuit

that computes timing error at transition times, such as that in claim 21. Nor is such a general statement motivation to modify Patel to include such a timing recovery circuit. Thus, the Applicant respectfully submits that claim 21 should be allowable.

CONCLUSION

The Applicant respectfully submits that the present application is in condition for allowance. The Applicant thanks the Examiner for his work in examining the application and the prior art. If the Examiner has any questions or the Applicants can be of any assistance, the Examiner is invited and encouraged to contact the Applicants at the number below.

The Commissioner is authorized to charge any necessary fees or credit any overpayment to the Deposit Account of MHM, Account No. 13-0017.

Respectfully submitted,

Date: November 2, 2006

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